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MHTL

INTEGRATED CIRCUITS MC660 SERIES

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INTEGRATED CIRCUITS

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NUMERICAL INDEX (Functions and Characteristics)

V_{CC} = 15 V ± 1.0 V, T_A = 25°C, Case 93

Function	Type -30 to + 75°C	Output Loading Factor Each Output	Propagation Delay t _{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
Expandable Dual 4-Input NAND Gate (active pullup)	MC660P	10	110	88/26 ①	3-8
Expandable Dual 4-Input NAND Gate (passive pullup)	MC661P	10	125	88/26 ①	3-10
Expandable Dual 4-Input Line Driver	MC662P	30	140	180/26 ①	3-20
Dual J-K Flip-Flop	MC663P	9	—	200	3-22
Master-Slave R-S Flip-Flop	MC664P	8	—	160	3-24
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Triple 3-Input NAND Gate (passive pullup)	MC670P	10	125	132/39 ①	3-12
Triple 3-Input NAND Gate (active pullup)	MC671P	10	110	132/39 ①	3-14
Quad 2-Input NAND Gate (active pullup)	MC672P	10	110	176/52 ①	3-18

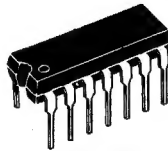
① Input High/Inputs Low

GENERAL INFORMATION

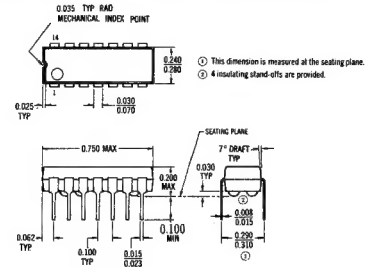
MHTL MC660 series

UNIBLOC® PLASTIC PACKAGE CASE 93

*Trademark of Motorola Inc.



TO-116



MAXIMUM RATINGS $T_A = 25^\circ\text{C}$

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, < 1.0 s	V_{CC}	18 20	Vdc
Input Voltage (MC669P Expanders Reverse Voltage)	V_{in}	-1.0/+18 18	Vdc
Output Current (into outputs) MC660, 661, 670, 671, 668, 672 MC662 MC663 MC664 MC669	—	30 60 28 26 —	mAdc
Input Reverse Current @ 20 V	I_R	0.5	mAdc
Forward Current (individual) MC669P	I_F	30	mAdc
Operating Temperature Range	T_A	-30 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$

TEST LIMITS TOLERANCE

$$T_A = \pm 3^\circ\text{C} \quad V_R = \pm 1\% \quad V_{CC} = \pm 1\% \quad V_{IL} = \pm 1\% \quad V_{IH} = \pm 1\% \quad V_F = \pm 1\% \quad I_{OL} = \pm 1\% \quad I_{OH} = \pm 1\%$$

DEFINITIONS

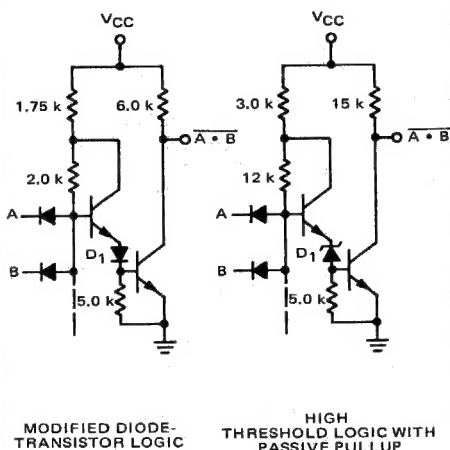
- CP Clock Pulse
- I_{CEX} Collector-to-emitter leakage of the output transistor
- I_{CCH} V_{CC} current drain when all inputs are high
- I_{CCL} V_{CC} current drain when all inputs are low
- I_F Forward current of input diodes for unit input load
- 2 I_F Forward current of input diodes which are equal to twice unit load
- I_{OH} Test current flowing into the output pin when output is high. (Negative)
- I_{OL} Test current flowing into output pin when output is low
- I_R Reverse current of input diodes with V_R applied
- 2 I_R Reverse current of two input diodes with V_R applied
- I_{SC} Short-circuit current obtained from device output when output is high

- t_{pd+} Propagation delay time for a positive-going output pulse
- t_{pd-} Propagation delay time for a negative-going output pulse
- V_{CC} Device power supply voltage
- V_{CCH} High power supply voltage
- V_{CCL} Low power supply voltage
- V_{CEX} Collector-to-emitter voltage of the output transistor
- V_F Input voltage when measuring I_F
- V_{IH} Threshold voltage for high input voltage state
- V_{IL} Threshold voltage for low input voltage state
- V_{OH} Output high voltage state with I_{OH} flowing out of pin
- V_{OL} Output low voltage state with I_{OL} flowing into pin
- V_R Reverse voltage for input diode leakage test
- V_X Threshold voltage for low input voltage state on expander unit

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
- The outputs of the passive pullup gates may be tied together to perform the wired-collector OR function. For each added gate subtract 1.2 output loading factor (fan-out).
- The outputs of the active pullup devices should not be tied together.

FIGURE 1—GATE COMPARISONS



HIGH THRESHOLD LOGIC

The High Threshold Logic (MHTL) family of integrated circuit devices was developed for applications requiring a higher degree of inherent electrical noise immunity than is available with the more standard forms of integrated circuit logic families. The basic MHTL logic gate is similar to the Diode Transistor Logic (MDTL) gate circuit as can be seen in Figure 1. A considerably larger input threshold characteristic is exhibited by the MHTL devices by using a reversed biased base-emitter junction which operates in the breakdown avalanche mode (sometimes referred to as zener operation) as compared to a forward biased diode junction for the corresponding D₁ element in the MDTL gate. A typical 7.5 volt input signal is required to turn on the MHTL output inverting transistor while a 1.5 volt signal is necessary for MDTL.

The higher threshold characteristic of MHTL requires a higher V_{CC} supply and is specified at 15 volts ±1.0 V tolerance. In order to keep the power dissipation within reasonable levels, higher values of resistance are used in MHTL than for corresponding resistors in the MDTL circuit. These resistance values also allow the outputs of gates to be interconnected to provide the "wired - or" logic function. The propagation delay of MHTL is in the order of 110 nanoseconds and consequently is a relatively slow logic family, a property which aids in rejecting noise. A comparison of transfer curves is made in Figure 2 illustrating the large logic swing available from MHTL.

An active output pullup configuration is available for the MHTL devices and is shown in Figure 3. The active output arrangement will allow the circuits to handle capacitive loads at a higher speed than is obtainable with the passive pullup configuration. Additionally, the impedance in the high state is considerably less, and consequently makes the family more immune to electrical noise. The active output configuration also allows for a more powerful arrangement to interface with discrete components.

In summary the MHTL devices may be characterized as an integrated circuit family with a high degree of inherent noise immunity, a high input threshold and a large logic swing. These characteristics make the line very attractive for use where electrical noise is an important consideration, as well as for applications where interfacing with various discrete components is required.

FIGURE 2—TRANSFER CURVES

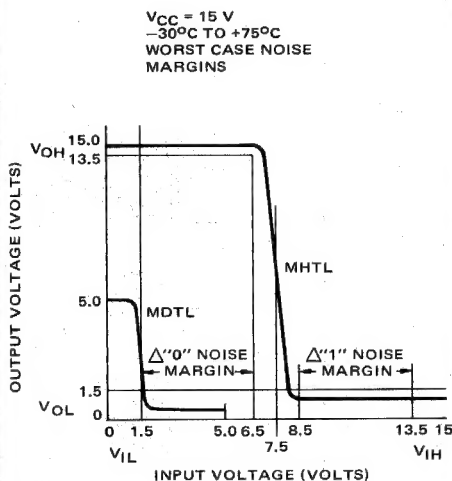
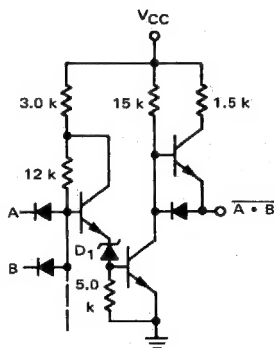


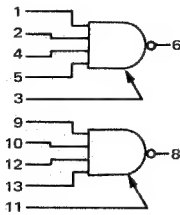
FIGURE 3—MHTL GATE WITH ACTIVE PULLUP



The logic diagrams shown describe the circuits of the MHTL line and permit quick selection of circuits required to implement a particular logic system. Pertinent information, such as logic equations and truth tables is

provided to show line compatibility. Package pin numbers and loading factors for each device are specified with each logic diagram. The numbers at the ends of the terminals are package pin numbers.

MC660P
EXPANDABLE
DUAL 4-INPUT GATE
(with active output pullup)

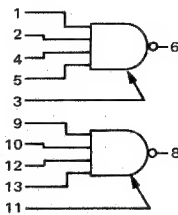


Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5} \cdot (3)$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 88 mW
Inputs Low - 26 mW

MC661P
EXPANDABLE
DUAL 4-INPUT GATE
(with passive output pullup)

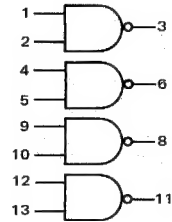


Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5} \cdot (3)$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 88 mW
Inputs Low - 26 mW

MC668P
QUAD 2-INPUT GATE
(with passive output pullup)

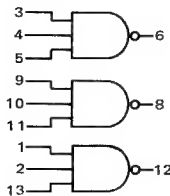


Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 176 mW
Inputs Low - 52 mW

MC670P
TRIPLE 3-INPUT GATE
(with passive output pullup)

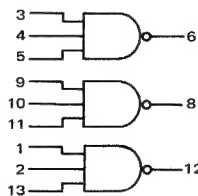


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 132 mW
Inputs Low - 39 mW

MC671P
TRIPLE 3-INPUT GATE
(with active output pullup)

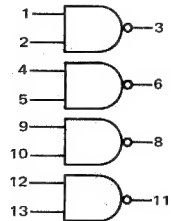


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 132 mW
Inputs Low - 39 mW

MC672P
QUAD 2-INPUT GATE
(with active output pullup)



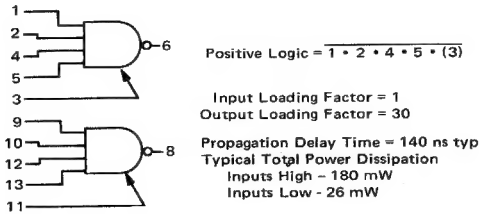
Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

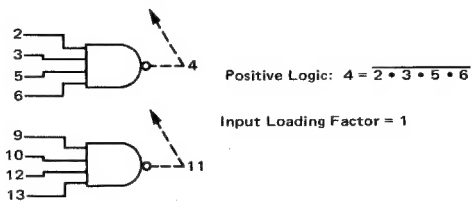
Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 176 mW
Inputs Low - 52 mW

LOGIC DIAGRAMS (continued)

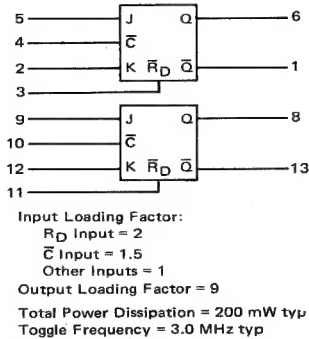
MC662P
EXPANDABLE
DUAL 4-INPUT LINE DRIVER
(with active output pullup)



MC669P
DUAL 4-INPUT EXPANDERS



MC663P
DUAL J-K FLIP-FLOP

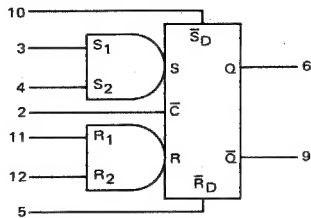


TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	\bar{Q}
0	0	Q_n	\bar{Q}_n
1	0	1	0
0	1	0	1
1	1	\bar{Q}_n	Q_n

Direct input (\bar{R}_D) must be high.
0 = low state
1 = high state
 t_n = time period prior to negative transition of clock pulse
 t_{n+1} = time period subsequent to negative transition of clock pulse
 Q_n = state of Q output in time period t_n
NOTE: A low state "0" at the direct reset \bar{R}_D causes a low state "0" at the Q output and the complement at the \bar{Q} output.

MC664P
MASTER-SLAVE R-S FLIP-FLOP



DIRECT INPUT
OPERATION

\bar{R}_D	\bar{S}_D	Q	\bar{Q}
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

CLOCKED OPERATION *

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

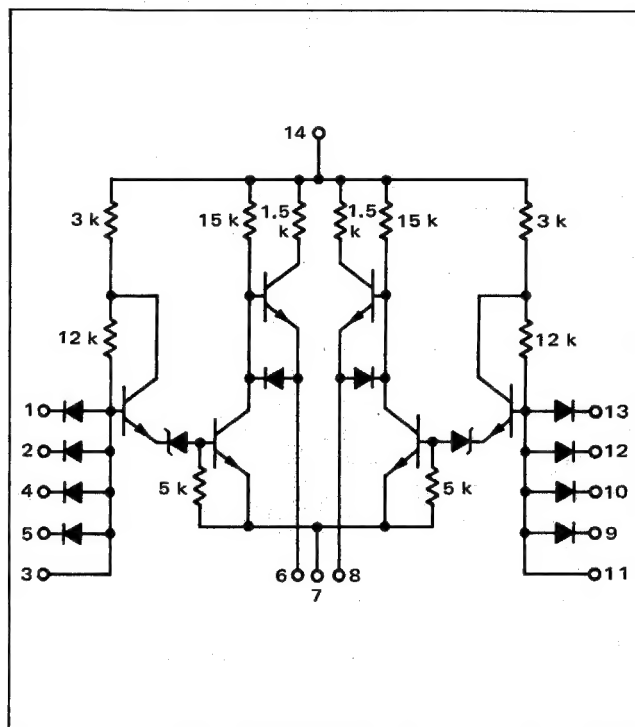
* Direct inputs (\bar{R}_D , \bar{S}_D) must be high.

0 = low state
1 = high state
NC = No change
NA = Not allowed
X = state of input does not affect state of the circuit
U = indeterminate state
 t_n = time period prior to negative transition of clock pulse
 t_{n+1} = time period subsequent to negative transition of clock pulse
 Q_n = state of Q output in time period t_n

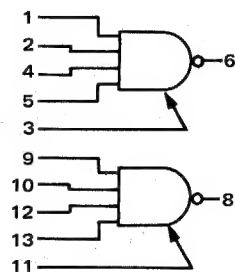
EXPANDABLE DUAL 4-INPUT GATE

MHTL MC660 series

MC660P



This device consists of two expandable 4-input NAND gates with active output pullup.

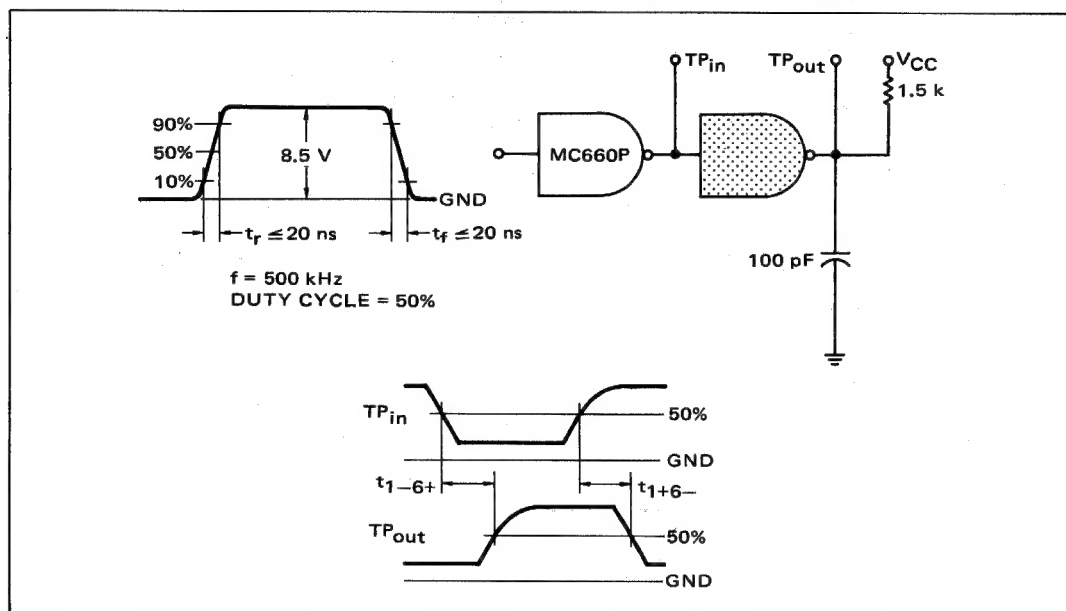


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 88 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gate is tested in the same manner.

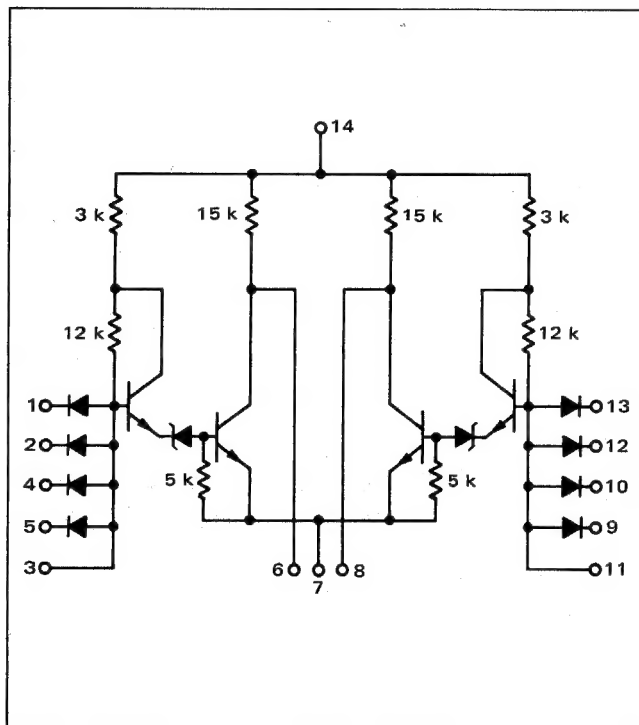
ELECTRICAL CHARACTERISTICS										TEST CURRENT/VOLTAGE VALUES (All Temperatures)											Gnd
										mA		Volts									
										I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _X	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
Characteristic	Symbol	Pin Under Test	TEST LIMITS						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
			-30°C		+25°C		+75°C			I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _X	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
			Min	Max	Min	Max	Min	Max													
Output Voltage	V _{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V _{OH}	6	-	-	12.5	-	12.5	-	↓	-	6	1	-	-	-	-	2, 4, 5	14	-	↓	
			-	-	↓	-	↓	-		-	↓	2	-	-	-	-	1, 4, 5	↓	-		
			-	-	-	-	-	-		-	↓	4	-	-	-	-	1, 2, 5	-	-		
			-	-	↓	-	↓	-		-	↓	5	-	-	3	-	1, 2, 4	↓	-	↓	
Short-Circuit Current	I _{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I _R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-	↓	-	↓	↓	-	-	-	-	-	2	-	-	-	-	1, 3, 4, 5, 7	
		4	-	-	-	-	-	-	↓	-	-	-	-	-	4	-	-	-	-	1, 2, 3, 5, 7	
		5	-	-	-	↓	-	↓	↓	-	-	-	-	-	5	-	-	-	↓	-	1, 2, 3, 4, 7
Output Leakage Current	I _{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6, 14	-	-	-	-	1, 7
Forward Current	I _F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-	↓	-	↓	↓	-	-	-	-	2	1, 4, 5	-	-	-	-	↓	↓
		4	-	-	-	-	-	-	↓	-	-	-	-	4	1, 2, 5	-	-	-	-	-	
		5	-	-	-	↓	-	↓	↓	-	-	-	-	5	1, 2, 4	-	-	-	-	↓	↓
Power Drain Current (Total Device)	I _{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I _{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times	t ₁₋₆₊ t ₁₊₆₋									Pulse In	Pulse Out										
		6	-	-	-	200	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
		6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

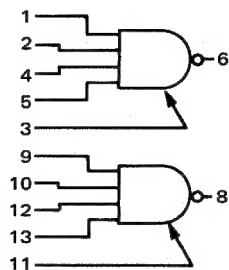
EXPANDABLE DUAL 4-INPUT GATE

MHTL MC660 series

MC661P



This device consists of two expandable 4-input NAND gates with passive output pullup.

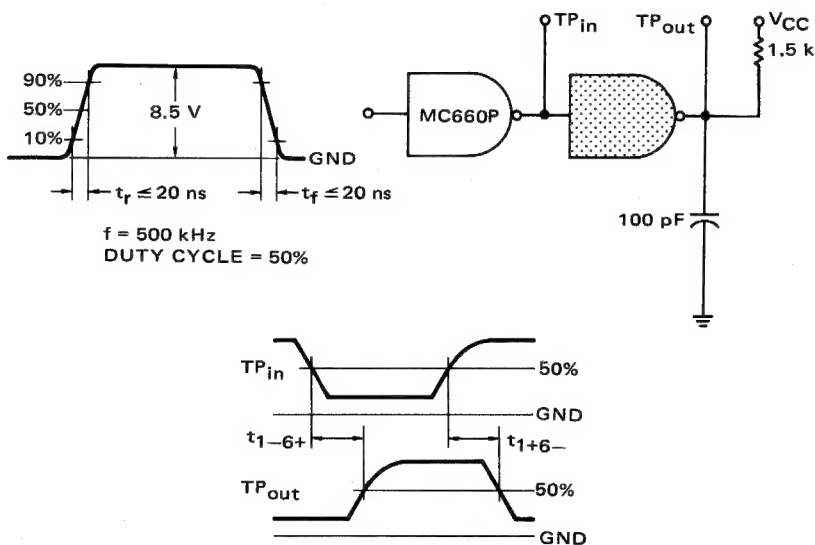


Positive Logic 6 = $\overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 88 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gate is tested in the same manner.

ELECTRICAL CHARACTERISTICS										TEST CURRENT/VOLTAGE VALUES (All Temperatures)											Gnd
										mA		Volts									
										I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _X	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
Characteristic	Symbol	Pin Under Test	TEST LIMITS						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
			-30°C		+25°C		+75°C			I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _X	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
Output Voltage	V _{OL}	6	-	1.5	-	1.5	-	1.5	V _{dc}	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V _{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-	-	-	-	-		-		2	-	-	-	-	-	1, 4, 5	-	-	
			-	-	-	-	-	-		-		4	-	-	-	-	-	1, 2, 5	-	-	
			-	-	-	-	-	-		-		5	-	-	-	-	-	1, 2, 4	-	-	
Short-Circuit Current	I _{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I _R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-	-	-	-		-	-	-	-	-	2	-	-	-	-	-	1, 3, 4, 5, 7
		4	-	-	-	-	-	-		-	-	-	-	-	4	-	-	-	-	-	1, 2, 3, 5, 7
		5	-	-	-	-	-	-		-	-	-	-	-	5	-	-	-	-	-	1, 2, 3, 4, 7
Output Leakage Current	I _{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I _F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-	-	-	-		-	-	-	-	2	1, 4, 5	-	-	-	-	-	
		4	-	-	-	-	-	-		-	-	-	-	4	1, 2, 5	-	-	-	-	-	
		5	-	-	-	-	-	-		-	-	-	-	5	1, 2, 4	-	-	-	-	-	
Power Drain Current (Total Device)	I _{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I _{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
										1	6										
										1	6										
	t ₁₋₆₊	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t ₁₊₆₋	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

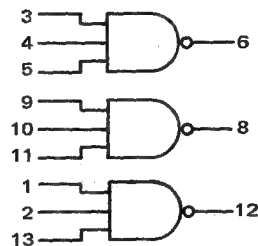
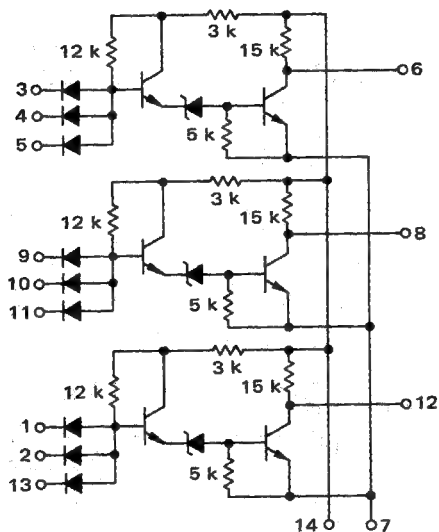
Pins not listed are left open.

TRIPLE 3-INPUT GATE

MHTL MC660 series

MC670P

This device consists of three 3-input NAND gates with passive output pull-up.



Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1

Output Loading Factor = 10

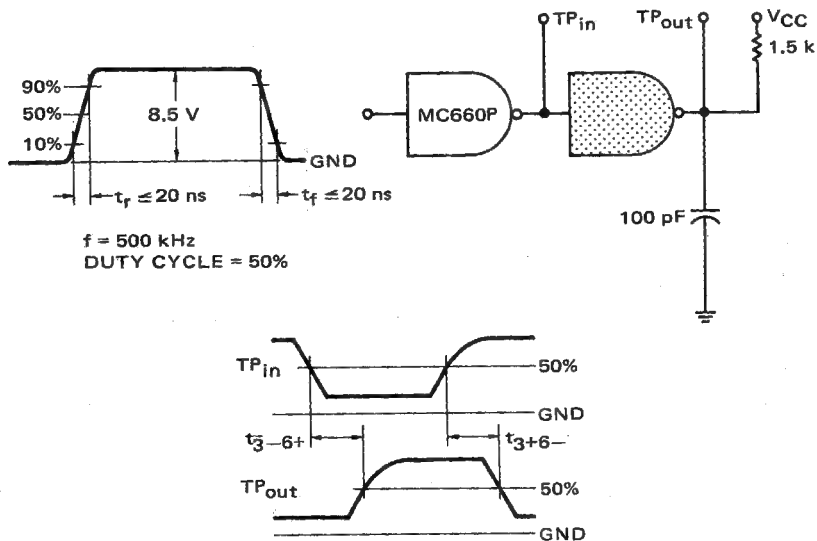
Propagation Delay Time = 125 ns typ

Typical Total Power Dissipation

Input High = 132 mW

Inputs Low = 39 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS										TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
Test procedures are shown for only one gate. The other gates are tested in the same manner.										mA		Volts								
										I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Characteristic	Symbol	Pin Under Test	TEST LIMITS						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										Gnd
			-30°C		+25°C		+75°C			I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
Output Voltage	V _{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3, 4, 5	-	-	-	-	14	-	7
	V _{OH}	6	-	-	12.5	-	12.5	-	↓	-	6	3	-	-	-	-	4, 5	14	-	↓
		↓	-	-	↓	-	↓	-		-	↓	4	-	-	-	3, 5	↓	-		
Short-Circuit Current	I _{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	3, 6, 7
Reverse Current	I _R	3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	14	-	4, 5, 7
		4	-	-	-	↓	-	↓	-	-	-	-	-	4	-	-	↓	-	3, 5, 7	
		5	-	-	-	↓	-	↓	↓	-	-	-	-	5	-	-	↓	-	3, 4, 7	
Output Leakage Current	I _{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6, 14	-	-	-	3, 7
Forward Current	I _F	3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	4, 5	-	-	-	14	7
		4	-	-	-	↓	-	↓	-	-	-	-	4	3, 5	-	-	-	↓	↓	
		5	-	-	-	↓	-	↓	↓	-	-	-	-	5	3, 4	-	-	-	↓	
Power Drain Current (Total Device)	I _{CCL}	14	-	-	-	4.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1, 2, 3, 4, 5, 7, 9, 10, 11, 13
	I _{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times	t ₃₋₆₊ t ₃₊₆₋								ns	Pulse In	Pulse Out									
										3	6									
										3	6									
									ns								14	-	-	7
									ns								14	-	-	7

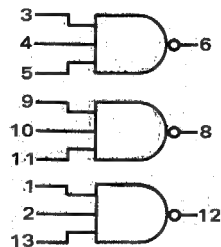
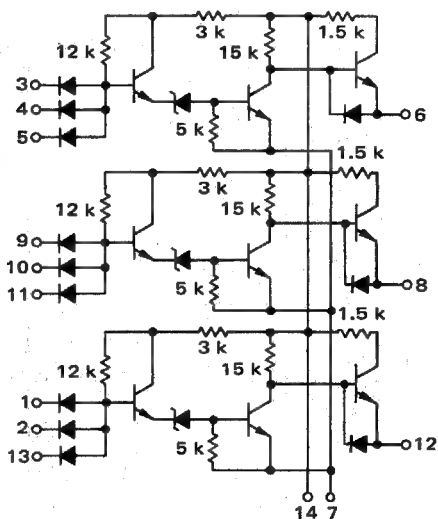
Pins not listed are left open.

TRIPLE 3-INPUT GATES

MHTL MC660 series

MC671P

This device consists of three 3-input NAND gates with active output pull-up.

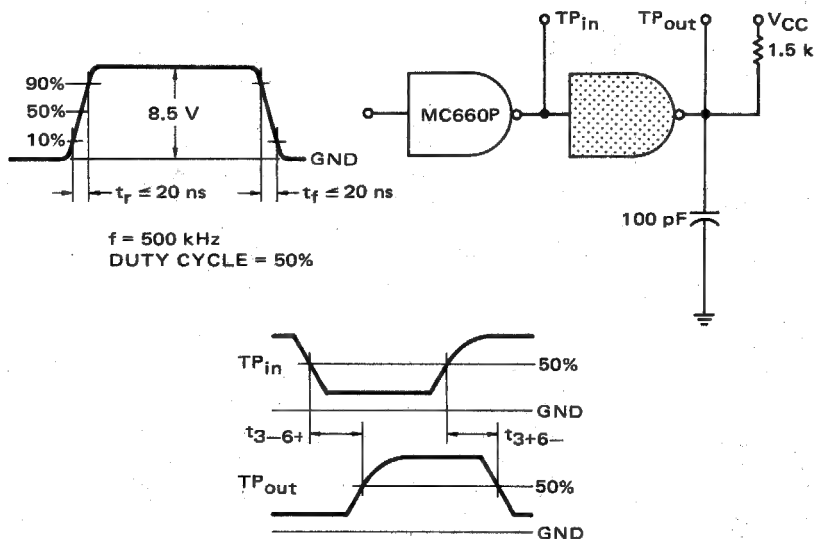


Positive Logic: $6 = 3 \cdot 4 \cdot 5$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 132 mW
Inputs Low = 39 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
mA		Volts							
I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0

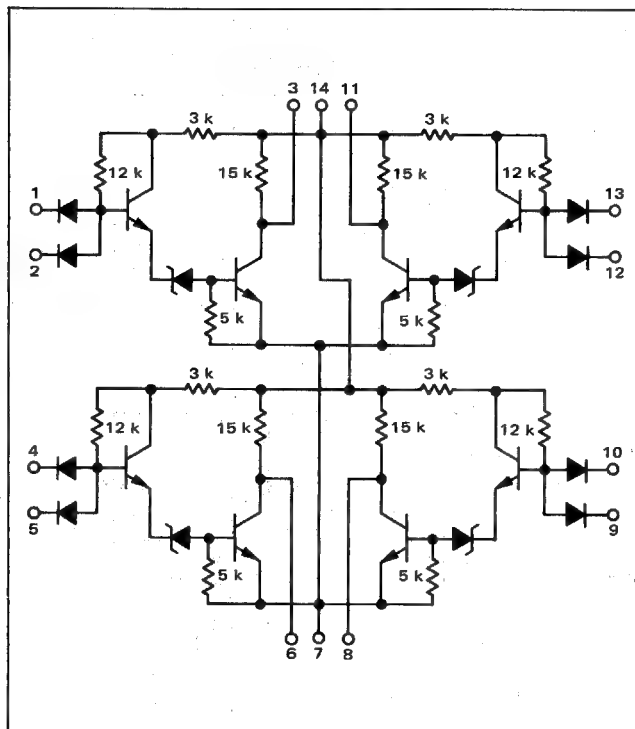
Characteristic	Symbol	Pin Under Test	TEST LIMITS						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Gnd
			-30°C		+25°C		+75°C			I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}		
			Min	Max	Min	Max	Min	Max													
Output Voltage	V _{OL}	6	-	1.5	-	1.5	-	1.5	V _{dC}	6	-	-	3, 4, 5	-	-	-	-	14	-	7	
	V _{OH}	6	-	-	12.5	-	12.5	-	V _{dC}	-	6	3	-	-	-	-	4, 5	14	-	↓	
		↓	-	-	↓	-	↓	-	↓	-	↓	4	-	-	-	-	3, 5	↓	-		
Short-Circuit Current	I _{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdC	-	-	-	-	-	-	-	-	-	14	3, 6, 7	
Reverse Current	I _R	3	-	-	-	2.0	-	2.0	μAdC	-	-	-	-	-	3	-	-	14	-	4, 5, 7	
		4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	-	-	3, 5, 7	
		5	-	-	-	↓	-	↓	↓	-	-	-	-	-	5	-	-	↓	-	3, 4, 7	
Output Leakage Current	I _{CEX}	6	-	-	-	100	-	100	μAdC	-	-	-	-	-	-	6, 14	-	-	-	3, 7	
Forward Current	I _F	3	-	-	-	-1.20	-	-1.20	mAdC	-	-	-	-	3	4, 5	-	-	-	14	7	
		4	-	-	-	↓	-	↓	↓	-	-	-	-	4	3, 5	-	-	-	↓	↓	
		5	-	-	-	↓	-	↓	↓	-	-	-	-	5	3, 4	-	-	-	↓	↓	
Power Drain Current (Total Device)	I _{CCL}	14	-	-	-	4.5	-	-	mAdC	-	-	-	-	-	-	-	-	-	14	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	
	I _{CCH}	14	-	-	-	15	-	-	mAdC	-	-	-	-	-	-	-	-	-	14	7	
Switching Times	t ₃₋₆₊ t ₃₊₆₋	6	-	-	-	200	-	-	ns	Pulse In	Pulse Out	-	-	-	-	-	14	-	-	7	
										3	6										
										3	6										
		6	-	-	-	100	-	-	ns	3	6	-	-	-	-	-	14	-	-	7	

Pins not listed are left open.

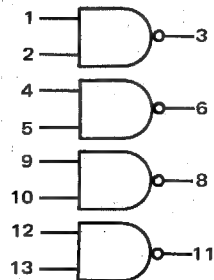
QUAD 2-INPUT GATES

MHTL MC660 series

MC668P



This device consists of four 2-input NAND gates with passive output pull-up.



Positive Logic: $3 = 1 \cdot 2$

Input Loading Factor = 1

Output Loading Factor = 10

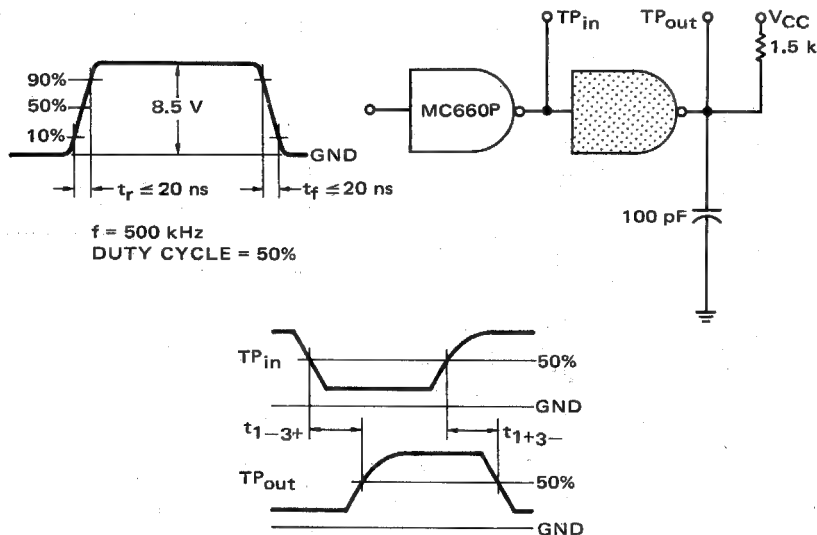
Propagation Delay Time = 125 ns typ

Typical Total Power Dissipation

Input High = 176 mW

Inputs Low = 52 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

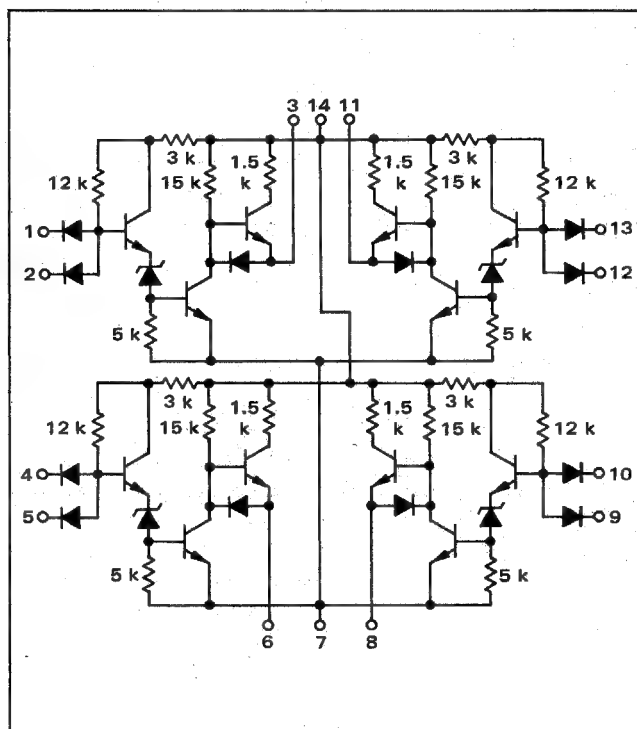
TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	Gnd
3	-	-	1, 2	-	-	-	-	14	-	7
-	3	1	-	-	-	-	2	14	-	↓
-	3	2	-	-	-	-	1	14	-	
-	-	-	-	-	-	-	-	-	14	1, 3, 7
-	-	-	-	-	1	-	-	14	-	2, 7
-	-	-	-	-	2	-	-	14	-	1, 7
-	-	-	-	-	-	3, 14	-	-	-	1, 7
-	-	-	-	1	2	-	-	-	14	7
-	-	-	-	2	1	-	-	-	14	7
-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
-	-	-	-	-	-	-	-	-	14	7
Pulse In	Pulse Out									
1	3	-	-	-	-	-	14	-	-	7
1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

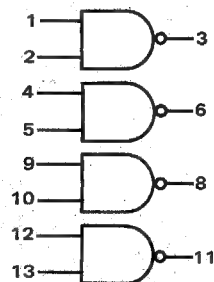
QUAD 2-INPUT GATES

MHTL MC660 series

MC672P



This device consists of four 2-input NAND gates with active output pull-up.



Positive Logic: $3 = 1 \cdot 2$

Input Loading Factor = 1

Output Loading Factor = 10

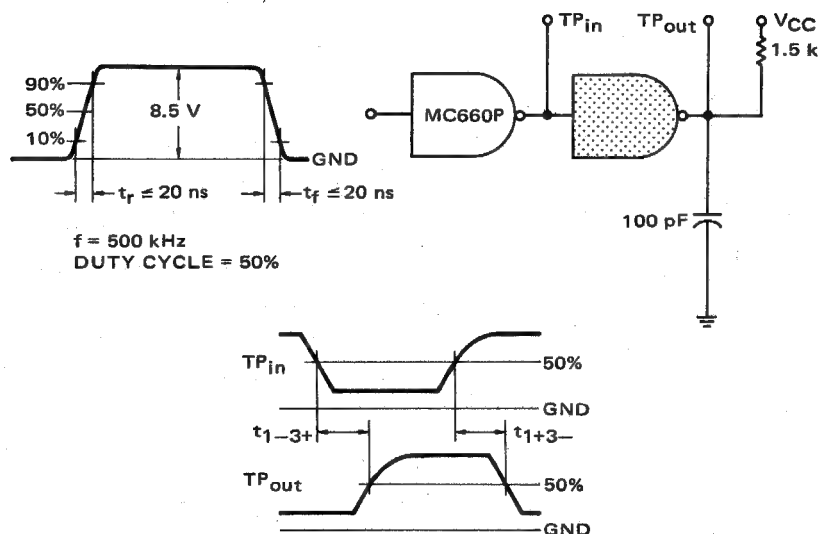
Propagation Delay Time = 110 ns typ

Typical Total Power Dissipation

Input High = 176 mW

Inputs Low = 52 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
The other gates are tested in the same manner.

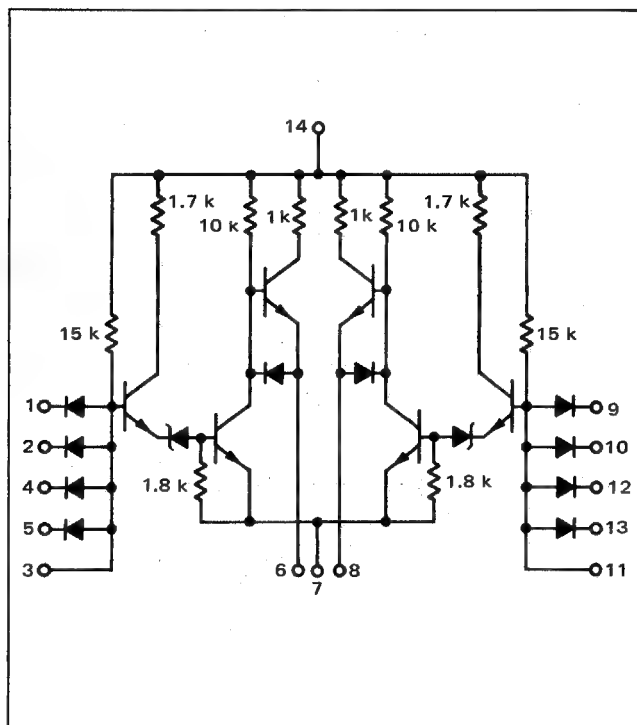
TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
mA		Volts									
I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}		
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0		
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
	I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}	Gnd
	3	-	-	1, 2	-	-	-	-	14	-	7
	-	3	1	-	-	-	-	2	14	-	7
	-	3	2	-	-	-	-	1	14	-	7
c	-	-	-	-	-	-	-	-	-	14	1, 3, 7
c	-	-	-	-	-	1	-	-	14	-	2, 7
c	-	-	-	-	-	2	-	-	14	-	1, 7
c	-	-	-	-	-	-	3, 14	-	-	-	1, 7
c	-	-	-	-	1	2	-	-	-	14	7
c	-	-	-	-	2	1	-	-	-	14	7
c	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9 10, 12, 13
c	-	-	-	-	-	-	-	-	-	14	7
	Pulse In	Pulse Out									
	1	3	-	-	-	-	-	14	-	-	7
	1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

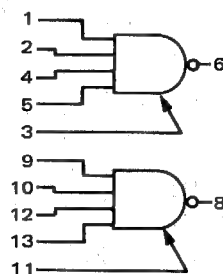
EXPANDABLE DUAL 4-INPUT LINE DRIVER

MHTL MC660 series

MC662P



This device consists of two expandable 4-input NAND line drivers with active output pullup. This device allows fan-out to 30 MHTL gates and drives large capacitive loads.

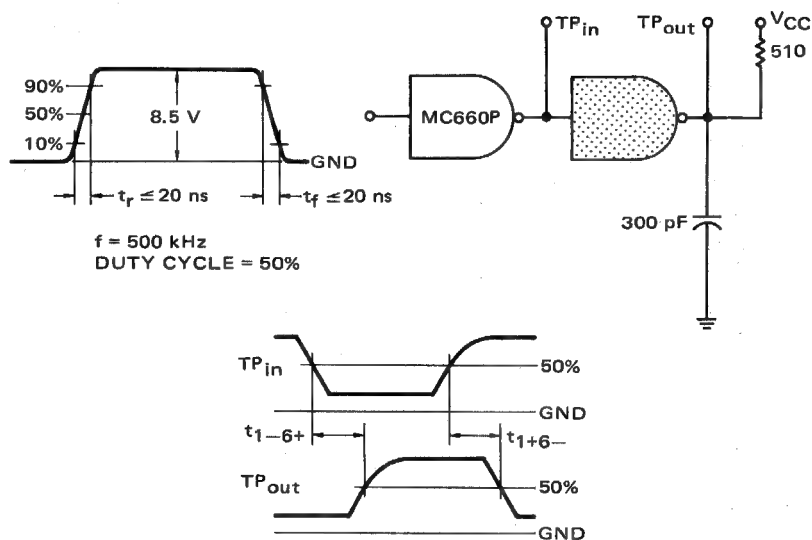


Positive Logic = $1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)$

Input Loading Factor = 1
Output Loading Factor = 30

Propagation Delay Time = 140 ns typ
Typical Total Power Dissipation
Input High = 180 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one driver only.
The other driver is tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)											Gnd	
mA		Volts										
I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _X	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}		
36.0	-0.09	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0		
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											Gnd	
I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _X	V _{CEX}	V _{CC}	V _{CCL}	V _{CCH}		
6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-		7
-	6	1	-	-	-	-	-	2, 4, 5	14	-		↓
-	↓	2	-	-	-	-	-	1, 4, 5	↓	-		
-		4	-	-	-	-	-	1, 2, 5	-	-		
-		5	-	-	-	-	-	1, 2, 4	↓	-		
-		-	-	-	-	3	-	-	-	-		
-	-	-	-	-	-	-	-	-	-	14	1, 6, 7	
-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7	
-	-	-	-	-	2	-	-	-	↓	-	1, 3, 4, 5, 7	
-	-	-	-	-	4	-	-	-	-	-	1, 2, 4, 5, 7	
-	-	-	-	-	5	-	-	-	↓	-	1, 2, 3, 4, 7	
-	-	-	-	-	-	-	6, 14	-	-	-	1, 7	
-	-	-	-	1	2, 4, 5	-	-	-	-	14	7	
-	-	-	-	2	1, 4, 5	-	-	-	-	↓	↓	
-	-	-	-	4	1, 2, 5	-	-	-	-	-		
-	-	-	-	5	1, 2, 4	-	-	-	-	↓		
-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7	
-	-	-	-	-	-	-	-	-	-	14	9, 10, 12, 13	
											7	
Pulse In	Pulse Out											
1	6	-	-	-	-	-	-	14	-	-	7	
1	6	-	-	-	-	-	-	14	-	-	7	

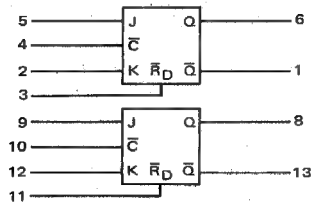
Pins not listed are left open.

DUAL J-K FLIP-FLOP

MHTL MC660 series

MC663P

Two J-K flip-flops in a single package. Each flip-flop has a direct reset input in addition to the clocked inputs.



TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	\bar{Q}
0	0	Q_n	\bar{Q}_n
1	0	1	0
0	1	0	1
1	1	\bar{Q}_n	Q_n

Input Loading Factor:

\bar{R}_D Input = 2

\bar{C} Input = 1.5

Other Inputs = 1

Output Loading Factor = 9

Loading factors are valid from -30°C to $+75^\circ\text{C}$
with $V_{CC} = 15 \pm 1 \text{ Vdc}$

$f_{Tog} = 3.0 \text{ MHz typ}$

Total Power Dissipation = 200 mW typ

Direct Input (\bar{R}_D) must be high.

0 = low state

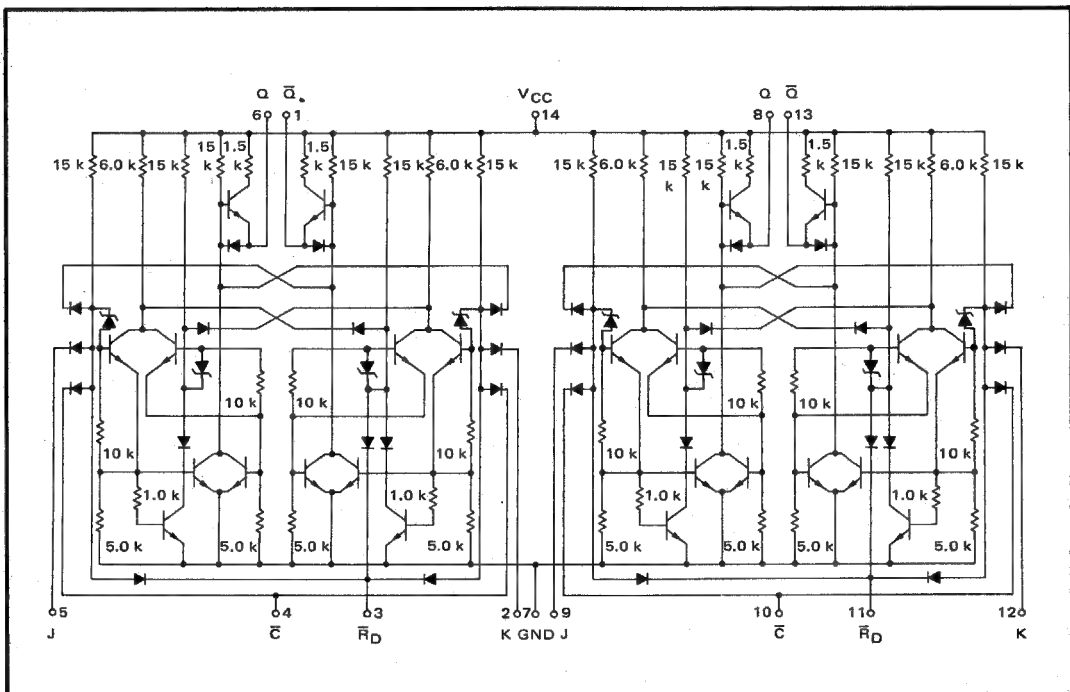
1 = high state

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset \bar{R}_D causes a low state "0" at the Q output and the complement at the \bar{Q} output.



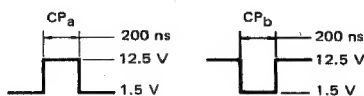
MC663P (continued)

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

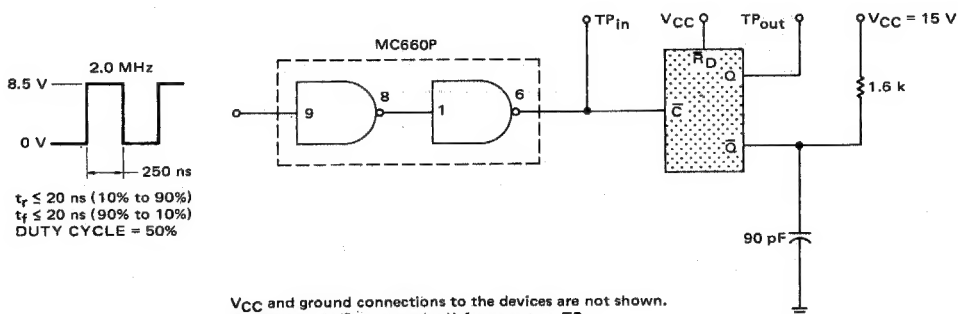
Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.										TEST CURRENT / VOLTAGE VALUES (All Temperatures)								CP _A	CP _B	Ground
										mA		Volts								
										I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CCL}	V _{CCH}			
										10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0			
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										
Characteristic	Symbol	Pin Under Test	TEST LIMITS						Unit											
			-30°C		+25°C		+75°C													
			Min	Max	Min	Max	Min	Max		I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CCL}	V _{CCH}			
Output Voltage	V _{OL}	1	-	1.5	-	1.5	-	1.5	V _{dc} ↓	1	-	2	3, 5	-	-	14	-	4	-	7
		6	-	1.5	-	1.5	-	1.5		6	-	5	2, 3	-	-	14	-	4	-	7
	V _{OH}	1	-	-	12.5	-	12.5	-		-	1	2, 3	5	-	-	14	-	4	-	7
		1	-	-	12.5	-	12.5	-		-	1	5	2, 3	-	-	14	-	4	-	7
		6	-	-	12.5	-	12.5	-		-	6	2	3, 5	-	-	14	-	4	-	7
Short-Circuit Current	I _{SC}	1	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	3, 4	-	-	-	-	14	-	-	1, 7
Reverse Current	I _R	2	-	-	-	2.0	-	2.0	μAdc ↓	-	-	-	-	-	2	14	-	-	-	3, 4, 5, 7
	3I _R	3	-	-	-	6.0	-	6.0		-	-	-	-	-	3	2, 4, 5, 14	-	-	-	7
	2I _R	4	-	-	-	4.0	-	4.0		-	-	-	-	-	4	14	-	-	-	2, 3, 5, 7
	I _R	5	-	-	-	2.0	-	2.0		-	-	-	-	-	5	14	-	-	-	2, 3, 4, 7
Forward Current	I _F	2	-	-	-	-1.20	-	-1.20	mAdc ↓	-	-	-	-	2	-	-	14	-	4	7
		3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	-	-	14	-	-	2, 4, 5, 7
	4	-	-	-	-1.20	-	-1.20	-		-	-	-	4	-	-	2, 5, 14	-	-	-	7
		5	-	-	-	-1.20	-	-1.20		-	-	-	-	5	-	-	14	-	4	7
Power Drain Current (Both Flip-Flops)	I _{CCL}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12
	I _{CCH}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.



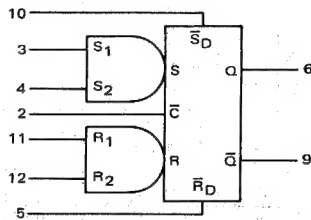
$t_r \leq 1.0 \mu s$ (10% to 90%)
 $t_f \leq 1.0 \mu s$ (90% to 10%)

TOGGLE MODE TEST CIRCUIT



MC664P

A dc coupled R-S flip-flop operating on the master-slave principle. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.



Input Loading Factor:
 C Input = 3
 Other Inputs = 1
 Output Loading Factor = 8
 Loading factors are valid from -30°C to $+75^{\circ}\text{C}$
 with $V_{CC} = 15 \pm 1 \text{ Vdc}$
 $f_{Tog} = 3.0 \text{ MHz typ}$
 Total Power Dissipation = 160 mW typ

DIRECT INPUT OPERATION

\bar{R}_D	\bar{S}_D	Q	\bar{Q}
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

NC = No change
 NA = Not allowed

CLOCKED OPERATION

		t_n		t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:

Direct inputs (\bar{R}_D , \bar{S}_D) must be high.

0 = low state

1 = high state

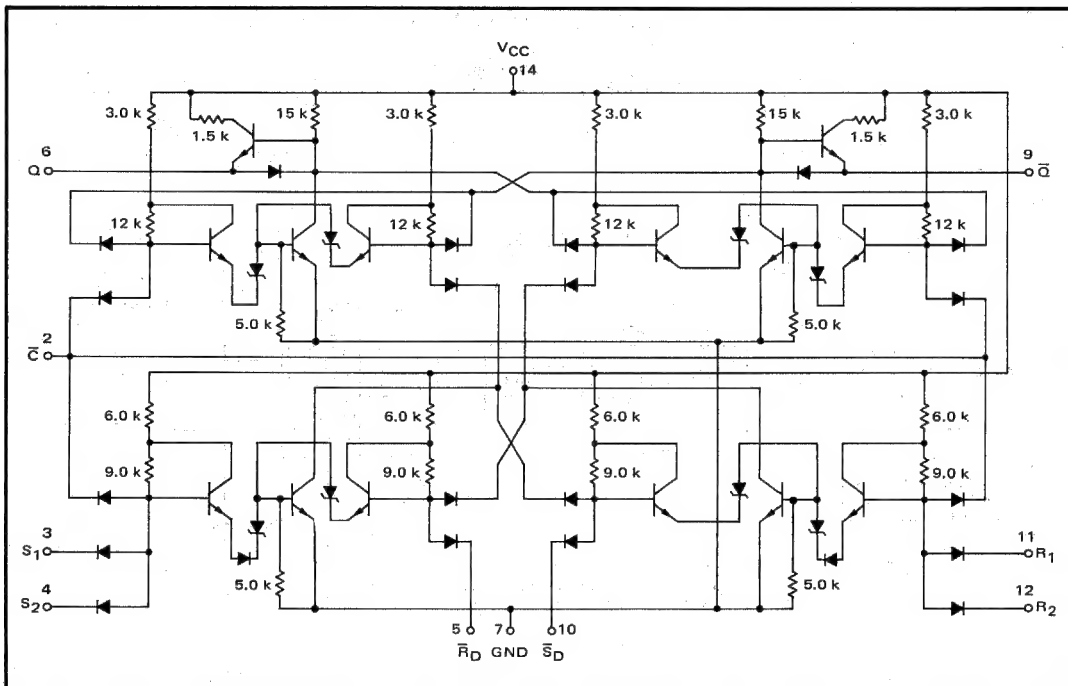
X = state of input does not affect state of the circuit

U = indeterminate state

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n



MC664P (continued)

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS										TEST CURRENT / VOLTAGE VALUES (All Temperatures)								CP _A	CP _B	Ground
										mA		Volts								
										I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CCL}	V _{CCH}			
										9, 6	-0.024	6, 5.0	8.50	1.5	16.0	14.0	16.0			
Characteristic	Symbol	Pin Under Test	TEST LIMITS						TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
			-30°C		+25°C		+75°C		Unit	I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _F	V _R	V _{CCL}	V _{CCH}			
			Min	Max	Min	Max	Min	Max												
Output Voltage	V _{OL}	6*	-	1.5	-	1.5	-	1.5	V _{dc}	6	-	-	3, 4, 11, 12	-	-	14	-	-	5	
		6	-	↓	-	↓	-	↓	6	-	4	3, 5, 11, 12	-	-	↓	-	2	7		
		6	-	↓	-	↓	-	↓	6	-	3	4, 5, 11, 12	-	-	↓	-	2	7		
		9‡	-	↓	-	↓	-	↓	9	-	-	3, 4, 11, 12	-	-	↓	-	10	7		
		9	-	↓	-	↓	-	↓	9	-	11	3, 4, 10, 12	-	-	↓	-	2	7		
	V _{OH}	9	-	↓	-	↓	-	↓	9	-	12	3, 4, 10, 11	-	-	↓	-	2	7		
		6	-	↓	12.5	-	12.5	-	↓	-	6	5	-	-	14	-	-	2, 3, 4, 7, 10, 11, 12		
		9	-	↓	12.5	-	12.5	-	↓	-	9	10	-	-	14	-	-	2, 3, 4, 5, 7, 11, 12		
Short-Circuit Current	I _{SC}	6	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 5	10	-	-	14	-	-	6, 7, 9	
		9	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 10	5	-	-	14	-	-	6, 7, 9	
Reverse Current	4I _{IR} 4I _{IR} I _R	2‡	-	-	-	8.0	-	8.0	μAdc	-	-	5	-	2	14	-	-	-	3, 4, 7, 10, 11, 12	
		2‡	-	-	-	8.0	-	8.0	μAdc	-	-	10	-	2	14	-	-	-	3, 4, 5, 7, 11, 12	
		3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	3	14	-	-	-	2, 4, 7	
		4	-	-	-	↓	-	↓	μAdc	-	-	-	-	4	14	-	-	-	2, 3, 7	
		5	-	-	-	↓	-	↓	μAdc	-	-	-	-	5	14	-	-	-	7	
		10	-	-	-	↓	-	↓	μAdc	-	-	2, 11, 12	-	10	14	-	-	-	2, 7, 12	
		11	-	-	-	↓	-	↓	μAdc	-	-	2, 3, 4	-	11	14	-	-	-	2, 7, 12	
		12	-	-	-	↓	-	↓	μAdc	-	-	-	-	12	14	-	-	-	2, 7, 11	
Forward Current	3I _F 3I _F I _F	2	-	-	-	-3.60	-	-3.60	mAdc	-	-	5	2	3, 4, 11, 12	-	14	-	-	7, 10	
		2	-	-	-	-3.60	-	-3.60	mAdc	-	-	10	2	3, 4, 11, 12	-	14	-	-	5, 7	
		3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	3	2, 4	-	14	-	-	7	
		4	-	-	-	↓	-	↓	mAdc	-	-	-	4	2, 3	-	14	-	-	7	
		5	-	-	-	↓	-	↓	mAdc	-	-	-	5	-	-	14	-	-	2, 7, 10, 11, 12	
		10	-	-	-	↓	-	↓	mAdc	-	-	-	10	-	-	14	-	-	2, 3, 4, 5, 7	
		11	-	-	-	↓	-	↓	mAdc	-	-	-	11	2, 12	-	14	-	-	7	
		12	-	-	-	↓	-	↓	mAdc	-	-	-	12	2, 11	-	14	-	-	7	
Power Drain Current	ICCL ICCH	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	14	-	-	2, 3, 4, 5, 7, 10, 11, 12	
		14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	14	-	-	7	

Pins not listed are left open.

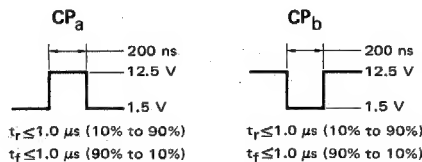
*Apply momentary ground to pins 9 and 10 prior to clock pulse

‡Apply momentary ground to pins 5 and 6 prior to clock pulse

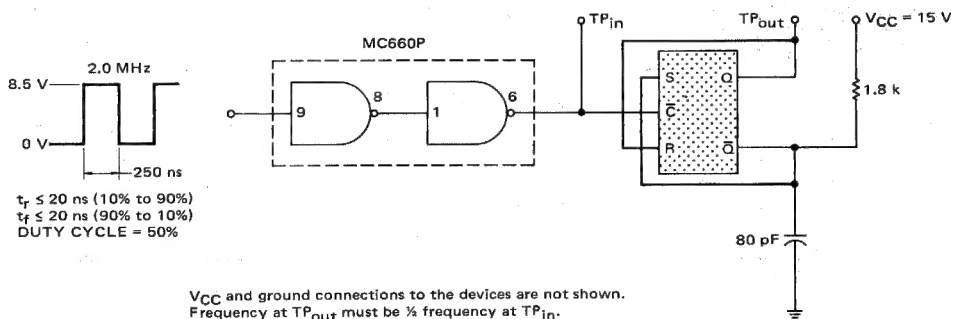
§Apply momentary ground to pin 9

†Apply momentary ground to pin 6

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100. 101. 102. 103. 104. 105. 106. 107. 108. 109. 110. 111. 112. 113. 114. 115. 116. 117. 118. 119. 120. 121. 122. 123. 124. 125. 126. 127. 128. 129. 130. 131. 132. 133. 134. 135. 136. 137. 138. 139. 140. 141. 142. 143. 144. 145. 146. 147. 148. 149. 150. 151. 152. 153. 154. 155. 156. 157. 158. 159. 160. 161. 162. 163. 164. 165. 166. 167. 168. 169. 170. 171. 172. 173. 174. 175. 176. 177. 178. 179. 180. 181. 182. 183. 184. 185. 186. 187. 188. 189. 190. 191. 192. 193. 194. 195. 196. 197. 198. 199. 200. 201. 202. 203. 204. 205. 206. 207. 208. 209. 210. 211. 212. 213. 214. 215. 216. 217. 218. 219. 220. 221. 222. 223. 224. 225. 226. 227. 228. 229. 230. 231. 232. 233. 234. 235. 236. 237. 238. 239. 240. 241. 242. 243. 244. 245. 246. 247. 248. 249. 250. 251. 252. 253. 254. 255. 256. 257. 258. 259. 260. 261. 262. 263. 264. 265. 266. 267. 268. 269. 270. 271. 272. 273. 274. 275. 276. 277. 278. 279. 280. 281. 282. 283. 284. 285. 286. 287. 288. 289. 290. 291. 292. 293. 294. 295. 296. 297. 298. 299. 300. 301. 302. 303. 304. 305. 306. 307. 308. 309. 310. 311. 312. 313. 314. 315. 316. 317. 318. 319. 320. 321. 322. 323. 324. 325. 326. 327. 328. 329. 330. 331. 332. 333. 334. 335. 336. 337. 338. 339. 340. 341. 342. 343. 344. 345. 346. 347. 348. 349. 350. 351. 352. 353. 354. 355. 356. 357. 358. 359. 360. 361. 362. 363. 364. 365. 366. 367. 368. 369. 370. 371. 372. 373. 374. 375. 376. 377. 378. 379. 380. 381. 382. 383. 384. 385. 386. 387. 388. 389. 390. 391. 392. 393. 394. 395. 396. 397. 398. 399. 400. 401. 402. 403. 404. 405. 406. 407. 408. 409. 410. 411. 412. 413. 414. 415. 416. 417. 418. 419. 420. 421. 422. 423. 424. 425. 426. 427. 428. 429. 430. 431. 432. 433. 434. 435. 436. 437. 438. 439. 440. 441. 442. 443. 444. 445. 446. 447. 448. 449. 450. 451. 452. 453. 454. 455. 456. 457. 458. 459. 460. 461. 462. 463. 464. 465. 466. 467. 468. 469. 470. 471. 472. 473. 474. 475. 476. 477. 478. 479. 480. 481. 482. 483. 484. 485. 486. 487. 488. 489. 490. 491. 492. 493. 494. 495. 496. 497. 498. 499. 500. 501. 502. 503. 504. 505. 506. 507. 508. 509. 510. 511. 512. 513. 514. 515. 516. 517. 518. 519. 520. 521. 522. 523. 524. 525. 526. 527. 528. 529. 530. 531. 532. 533. 534. 535. 536. 537. 538. 539. 540. 541. 542. 543. 544. 545. 546. 547. 548. 549. 550. 551. 552. 553. 554. 555. 556. 557. 558. 559. 560. 561. 562. 563. 564. 565. 566. 567. 568. 569. 570. 571. 572. 573. 574. 575. 576. 577. 578. 579. 580. 581. 582. 583. 584. 585. 586. 587. 588. 589. 590. 591. 592. 593. 594. 595. 596. 597. 598. 599. 600. 601. 602. 603. 604. 605. 606. 607. 608. 609. 610. 611. 612. 613. 614. 615. 616. 617. 618. 619. 620. 621. 622. 623. 624. 625. 626. 627. 628. 629. 630. 631. 632. 633. 634. 635. 636. 637. 638. 639. 640. 641. 642. 643. 644. 645. 646. 647. 648. 649. 650. 651. 652. 653. 654. 655. 656. 657. 658. 659. 660. 661. 662. 663. 664. 665. 666. 667. 668. 669. 670. 671. 672. 673. 674. 675. 676. 677. 678. 679. 680. 681. 682. 683. 684. 685. 686. 687. 688. 689. 690. 691. 692. 693. 694. 695. 696. 697. 698. 699. 700. 701. 702. 703. 704. 705. 706. 707. 708. 709. 710. 711. 712. 713. 714. 715. 716. 717. 718. 719. 720. 721. 722. 723. 724. 725. 726. 727. 728. 729. 730. 731. 732. 733. 734. 735. 736. 737. 738. 739. 740. 741. 742. 743. 744. 745. 746. 747. 748. 749. 750. 751. 752. 753. 754. 755. 756. 757. 758. 759. 760. 761. 762. 763. 764. 765. 766. 767. 768. 769. 770. 771. 772. 773. 774. 775. 776. 777. 778. 779. 780. 781. 782. 783. 784. 785. 786. 787. 788. 789. 790. 791. 792. 793. 794. 795. 796. 797. 798. 799. 800. 801. 802. 803. 804. 805. 806. 807. 808. 809. 810. 811. 812. 813. 814. 815. 816. 817. 818. 819. 820. 821. 822. 823. 824. 825. 826. 827. 828. 829. 830. 831. 832. 833. 834. 835. 836. 837. 838. 839. 840. 84



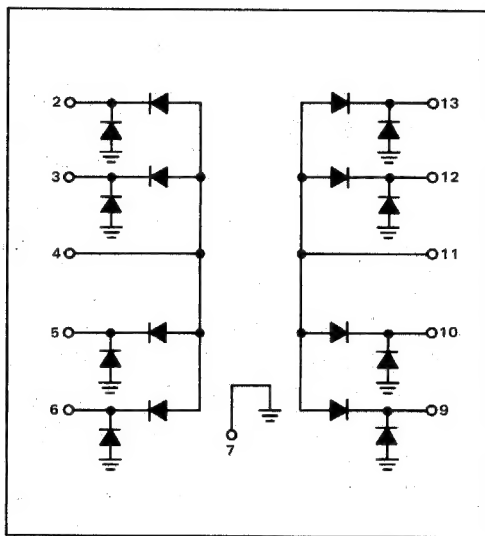
TOGGLE MODE TEST CIRCUIT



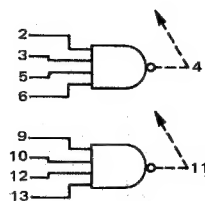
DUAL 4-INPUT EXPANDERS

MHTL MC660 series

MC669P



This device consists of two independent high voltage diode networks with characteristics matched to the input of the gate and buffer elements in the MHTL logic family. Its use increases the fan-in capability of other MHTL devices to a maximum of 20 while having negligible effect on their performance.



Positive Logic: $4 = 2 \cdot 3 \cdot 5 \cdot 6$

Input Loading Factor = 1

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander.
The other expander is tested in the same manner.

| Characteristic | Symbol | Pin Under Test | TEST LIMITS | | | | | | Unit | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: | | |
|-----------------|------------------|----------------|-------------|----------|-------|----------|-------|----------|-----------------------|--|------------------|------------------------------|
| | | | -30°C | | +25°C | | +75°C | | | I _F | V _R | Gnd |
| | | | Min | Max | Min | Max | Min | Max | | | | |
| Forward Voltage | V _F | 4
↓ | - | 1.0
↓ | - | 0.9
↓ | - | 0.8
↓ | V _{dc}
↓ | 4
↓ | -
-
-
- | 2, 7
3, 7
5, 7
6, 7 |
| Reverse Current | I _R | 2 | - | 2.0 | - | 2.0 | - | 2.0 | μA _{dc}
↓ | - | 2 | 3, 5, 6, 7 |
| | | 3 | - | ↓ | - | ↓ | - | ↓ | | - | 3 | 2, 5, 6, 7 |
| | | 5 | - | ↓ | - | ↓ | - | ↓ | | - | 5 | 2, 3, 6, 7 |
| | | 6 | - | ↓ | - | ↓ | - | ↓ | | - | 6 | 2, 3, 5, 7 |
| | 2 I _R | 4 | - | - | - | 4.0 | - | - | | - | 4 | 7 |

Pins not listed are left open